

What is claimed is:

- 1        1.    An apparatus, comprising:  
2            a first block to process a P-type frame in a  
3 video bitstream using a first error resilience technique;  
4 and  
5            a second block to process a B-type frame in the  
6 video bitstream using a second error resilience technique,  
7 wherein the first error resilience technique is different  
8 from the second error resilience technique.
- 1        2.    The apparatus of claim 1, wherein the first block  
2 further processes an I-type frame.
- 1        3.    The apparatus of claim 1, wherein the second  
2 block comprises a resynchronization marking block.
- 1        4.    The apparatus of claim 3, wherein the second  
2 block comprises a variable length coder block.
- 1        5.    The apparatus of claim 1, wherein the first block  
2 applies resynchronization markers to the video bitstream at  
3 a first interval and the second block applies  
4 resynchronization markers to the video bitstream at a  
5 second interval, wherein the second interval is longer than  
6 the first interval.

1        6. The apparatus of claim 1, wherein the second  
2 block inserts fewer error resilience bits in the video  
3 bitstream than the first block.

1        7. The apparatus of claim 1, further comprising a  
2 third block to process the P-type frame using a first error  
3 concealment technique.

1        8. The apparatus of claim 7, further comprising a  
2 fourth block to process the B-type frame using a second  
3 error concealment technique, wherein the first error  
4 concealment technique is different from the second error  
5 concealment technique.

1        9. The apparatus of claim 1, wherein the first block  
2 comprises:

3            a data partitioning block having an input  
4 terminal and an output terminal;

5            a reversible variable length coder block having  
6 an input terminal and an output terminal, wherein the  
7 output terminal of the data partitioning block is coupled  
8 to the input terminal of the reversible variable length  
9 code block;

10           a header extension code block having an input  
11 terminal and an output terminal, wherein the output  
12 terminal of the reversible variable length code block is  
13 coupled to the input terminal of the header extension code  
14 block; and

15           a resynchronization marker block having an input  
16 terminal and an output terminal, wherein the output

17 terminal of the header extension code block is coupled to  
18 the input terminal of the resynchronization marker block.

1       10. An article comprising one or more machine-  
2 readable storage media containing instructions that when  
3 executed enables a processor to:  
4           receive a video stream having at least a first  
5 type of frame and a second type of frame; and  
6           process the first type of frame using a first  
7 error resilience technique and the second type of frame  
8 using a second error resilience technique, wherein the  
9 first error resilience technique comprises applying  
10 resynchronization markers to the video stream at a selected  
11 interval and the second error resilience technique  
12 comprises applying resynchronization markers at an interval  
13 different from the selected interval.

1       11. The article of claim 10, wherein the instructions  
2 when executed enable the processor to process a P-type  
3 frame using the first error resilience technique.

1       12. The article of claim 11, wherein the instructions  
2 when executed enable the processor to process a B-type  
3 frame using the second error resilience technique.

1       13. The article of claim 12, wherein the instructions  
2 when executed enable the processor to process the B-type  
3 frame using a simpler error resilience technique than the  
4 P-type frame.

1        14. The article of claim 13, wherein the instructions  
2 when executed enable the processor to insert  
3 resynchronization markers in the video stream at a first  
4 pre-selected interval for the B-type frame and at a second  
5 pre-selected interval for the P-type frame, wherein the  
6 first pre-selected interval is longer than the second pre-  
7 selected interval.

1        15. The article of claim 10, wherein the instructions  
2 when executed enable the processor to process the first  
3 type of frame using a first error concealment technique and  
4 the second type of frame using a second error concealment  
5 technique, wherein the first error concealment technique is  
6 different from the second error concealment technique.

1        16. The article of claim 10, wherein the instructions  
2 when executed enable the processor to insert fewer error  
3 resilience bits into the video stream for the B-type frame  
4 than for the P-type frame.

1        17. The article of claim 10, wherein the instructions  
2 when executed enable the processor to perform variable  
3 length coding on the B-type frame.

1        18. The article of claim 10, wherein the instructions  
2 when executed enable the processor to apply  
3 resynchronization markers to the video for the B-type  
4 frame.

1        19. An apparatus, comprising:  
2            a first block to process a P-type frame in an  
3 encoded bitstream using a first error concealment  
4 technique; and  
5            a second block to process a B-type frame in the  
6 encoded video bitstream using a second error concealment  
7 technique, wherein the first error concealment technique is  
8 different from the second concealment technique.

1        20. The apparatus of claim 19, wherein the second  
2 block comprises a variable length decoder block.

1        21. The apparatus of claim 19, wherein the second  
2 error concealment technique comprises performing a block  
3 copy.

1        22. A method comprising:  
2            receiving a video stream;  
3            performing error resilience on a P-type frame  
4 within the video stream using a first technique; and  
5            performing error resilience on a B-type frame  
6 within the video stream using a second technique, wherein  
7 the first technique is different from the second technique.

1        23. The method of claim 22, further comprising  
2 performing error resilience on an I-type frame.

1        24. The method of claim 22, wherein the first  
2 technique comprises applying resynchronization markers to  
3 the video bitstream at a first interval and the second

4 technique comprises applying resynchronization markers at a  
5 second interval, wherein the second interval is longer than  
6 the first interval.

1 25. The method of claim 22, wherein the second  
2 technique inserts fewer error resilience bits in the video  
3 bitstream than the first error resilience technique.

1 26. The method of claim 22, further including  
2 performing error concealment on the P-type frame using a  
3 first technique and performing error concealment on the B-  
4 type frame using a second technique, wherein the first  
5 technique is different from the second technique.

1 27. An apparatus, comprising:  
2 a first block to perform error concealment on an  
3 encoded video signal and provide an output signal;  
4 a second block to determine at least one channel  
5 characteristic; and  
6 a third block to perform error resilience on the  
7 output signal based on the at least one channel  
8 characteristic and provide a modified video signal.

1 28. The apparatus of claim 27, further comprising at  
2 least of a block to transmit the modified signal and to  
3 store the modified signal to a storage device.

1 29. The apparatus of claim 27, wherein the third  
2 block performs error resilience on a P-type frame using a  
3 first technique and on a B-type frame using a second

4 technique, wherein the first technique is different from  
5 the second technique.

1 30. The apparatus of claim 27, wherein the first  
2 block performs error concealment on a P-type frame using a  
3 first technique and on a B-type frame using a second  
4 technique, wherein the first technique is different from  
5 the second technique.